ANALYSIS OF SWITCH PERFORMANCE ON THE MERCURY PULSED-POWER GENERATOR*

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Abstract

Mercury, Figure 1, is a magnetically-insulated inductive voltage adder that was acquired, assembled, and made operational by the Pulsed Power Physics Branch at the Naval Research Laboratory in Washington, DC[1,2]. Mercury is designed to produce a 50-ns pulse of 6-MV peak voltage, and 360-kA peak current when operated at full power. This is accomplished using four, SF_6 filled, laser-triggered switches (LTSs) to transfer energy from four intermediate-storage capacitors to 12 pulse forming lines (PFLs). By discharging the PFLs in a parallel/series configuration via self-break water output switches (OSs) into six induction cells, the output pulse is realized. To achieve optimal power flow, OS closure times should be staggered according to the delay time between adjacent induction cavities[3]. Consequently, both LTS and OS jitter need to be kept to a minimum. During different stages of assembly, the LTSs and the OSs were tested using dummy loads[3]. This document will review the results of these tests.

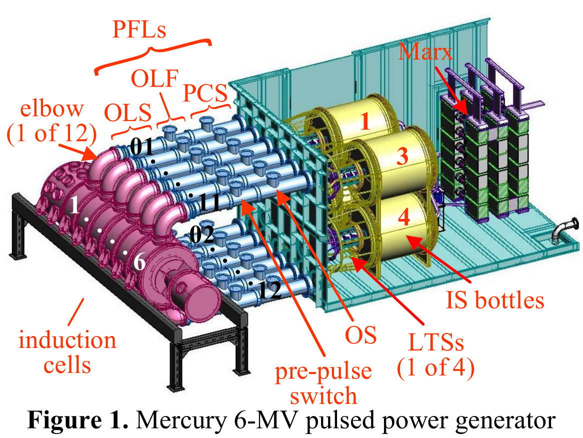

Figure 1. Mercury 6-MV pulsed power generator

I. INTRODUCTION

For Mercury (see Fig. 1) to achieve operational condition, several pulsed power tests were conducted at different stages of assembly[3]. The main motivation for conducting these initialization tests (279 total shots) prior to full machine operation was to avoid damaging the induction cells while determining machine operational parameters (LTS pressure and OS gap settings) and Marx charge levels. Additionally, the arrival of the PFL output pulses to their corresponding cell should be staggered in order to compensate for 2-ns cell-to-cell transit time. If the output pulses from each PFL do not arrive at their respective induction cells at the proper times, damaging over-voltages or reversals could result. As a result of these initialization tests, we determined that achievement of ideal cell-to-cell timing would be marginal given that the combined jitter of the LTSs and OSs was on the order of the desired cell-to-cell delay.

A. Technique Used for Staggering PFL Output Pulses

Mercury's architecture makes a straightforward approach to achieving proper PFL output pulse timings difficult. As shown in Figure 2, each cell is fed by two PFLs (i.e. PFLs 1 & 2 to Cell 1) and each IS bottle feeds three PFLs (i.e. IS 1 to PFLs 1, 3, & 5). Therefore, a portion of the charge from two different IS bottles feeds each cell. Due to this architecture, a combination of optical and OS closure time delays must be used to try to achieve the desired 2-ns delay between PFL output pulses.

1) Optical Delay

Figure 3 is a schematic of the trigger-laser-beam path, with the machine tank that houses the Marx, IS bottles, and LTSs shown as a reference. After the Marx erects and charges the IS bottles, the trigger laser is fired, triggering the LTSs. When the LTSs close, the IS bottles charge the "pulse charging section" (PCS) of each PFL to which they are connected (Fig. 1). The time the beam arrives at each LTS can be adjusted optically. This effectively adds delay between the time the PCS sections of PFLs 1-6 and PFLs 7-12 are charged. Hardware constraints limit this delay time to a maximum of 5.2ns, although the desired delay time is 6ns.

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14. ABSTRACT
Mercury, Figure 1, is a magnetically-insulated inductive voltage adder that was acquired, assembled, and made operational by the Pulsed Power Physics Branch at the Naval Research Laboratory in Washington, DC1,2. Mercury is designed to produce a 50-ns pulse of 6-MV peak voltage, and 360-kA peak current when operated at full power. This is accomplished using four, SF6 filled, laser-triggered switches (LTSs) to transfer energy from four intermediate-storage capacitors to 12 pulse forming lines (PFLs). By discharging the PFLs in a parallel/series configuration via self-break water output switches (OSs) into six induction cells, the output pulse is realized. To achieve optimal power flow, OS closure times should be staggered according to the delay time between adjacent induction cavities3. Consequently, both LTS and OS jitter need to be kept to a minimum. During different stages of assembly, the LTSs and the OSs were tested using dummy loads3. This document will review the results of these tests.

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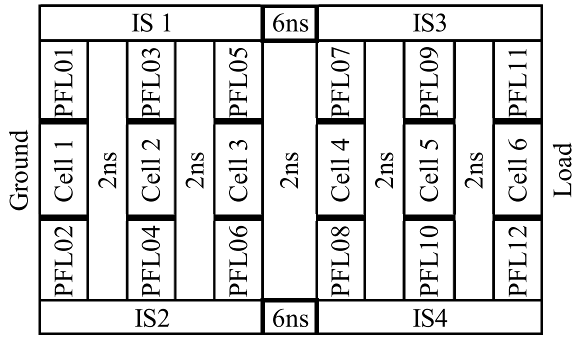

Figure 2. Diagram illustrating connection scheme from IS bottles to cells and ideal cell-to-cell and IS bottle-to-IS bottle delay times. In practice, IS bottles 3 and 4 are triggered 5.2ns after IS bottles 1 and 2.

2) OS Closure Delay

At some value of the PCS voltage, depending on the OS gap, the OS closes and the stored charge begins to transfer to the "output line first" (OLF) portion of the PFL. Prepulse coupled through the OS is reduced significantly by the prepulse switch as the output pulse travels to the "output line second" (OLS) portion of the PFL and onto the induction cell (Fig. 1). After the LTSs are triggered, the only remaining method to adjust PFL output pulse timings is to increase or reduce the OS gaps in each PFL. During PFL dummy-load tests (summary of results follows), it was found that an increase in OS gap length of 1mm corresponded to a 2ns delay in OS closure.

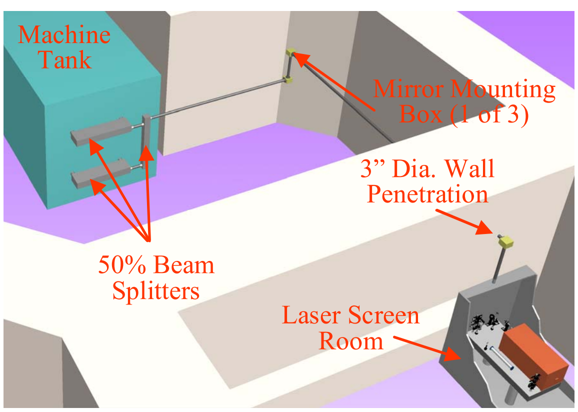

Figure 3. Mercury trigger laser beam path (PFLs and IVA not shown)

B. Calculated Effects of Staggering PFL Output Pulses

Simulations were performed using CASTLE (a circuit code developed at NRL) for three different operating conditions, all with an effective self-limited (22Ω) load. The results are shown in Figure 4. The load voltage and voltage across the insulator stacks in each cell are plotted for the three cases, all simulated assuming a 75-kV Marx charge. The first case shows what should be expected if all OSs closed at the same time (i.e. no optical or OS gap delay with no jitter). This case produces the worst results; stressing the insulator in cell 6 to 1.7MV at the peak and stressing all cell insulators differently. The second case illustrates the effect optical delay has on the system. Under this configuration (where OSs in PFLs 1-6 close 5.2ns before the OSs in PFLs 7-12, again with no jitter), a peak voltage of 1.6MV across the insulators in cells 3 and 6 is seen. The last case demonstrates how the insulators would be stressed if the machine were fired with no switch jitter when configured with 5.2-ns optical and successive 2-ns OS gap delays. A peak voltage level of approximately 1.4MV is seen across all insulators for this case.

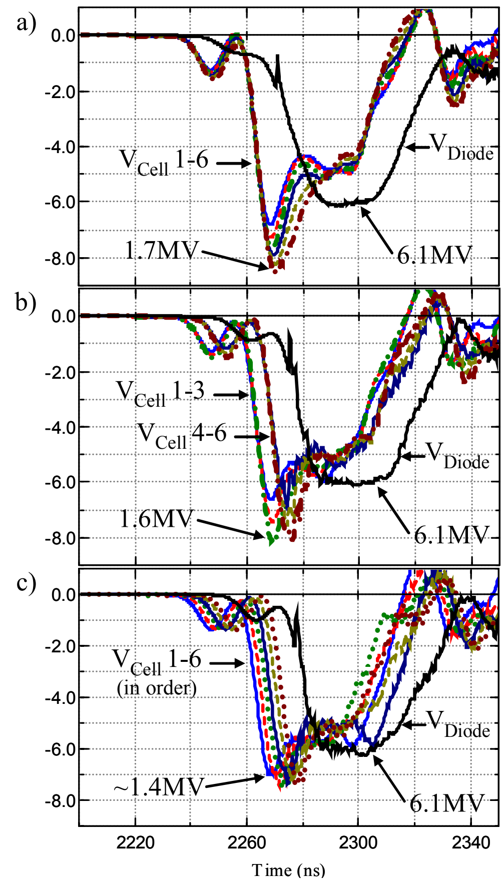

Figure 4. Results of Castle simulations of three different configurations (all plots have the same horizontal axis): a) no delay, b) optical delay, c) optical and OS gap delay

II. SWITCH PERFORMANCE ASSESSMENT

A. Jitter Calculation Techniques

A standardized method was chosen to characterize timing error for both the LTSs and OSs. This timing error, referred to commonly as jitter, was calculated by recording the time of steepest slope (switch closure) for all diagnostics of interest (the IS v-dot monitors in the case of the LTSs and the OLS v-dot monitors in the case of the OSs). The standard deviation for all four LTS closure times was calculated yielding the LTS jitter for that shot. An average of these LTS jitters over a specific range of shots is then taken to arrive at a single number

for LTS jitter for that shot range. Calculating jitter for the OSs required removing the effects of the LTSs from the calculation. For this reason, OS closure times were grouped according to the IS bottle that fed the corresponding OSs (i.e. IS bottle 1 feeds PFLs 1, 3, and 5, therefore OS closure times for OS1, OS3, and OS5 were grouped together). OS jitter includes the effects of both the OS and pre-pulse switch because the OS closure time was measured at the OLS v-dot location (Figure 1). A jitter was calculated for each subgroup, resulting in four values of OS jitter per shot. An average of all of the OS jitters over the subgroups and over the range of shots of interest is then taken to arrive at a single number for OS jitter. All hardware delays were accounted for when calculating statistics for each shot.

B. PFL Dummy Load Tests and OS Performance

After an initial laser system check, the PFL dummy loads were installed and high-voltage tests were performed on all components from the Marx up to the outputs of the PFLs[3]. As shown in Figure 5, the elbows connecting each PFL to its respective cell were disconnected from the cell, the uppers (1, 3, 5, 7, 9, & 11) turned upward, the elbow center conductor replaced with an electrode, and the elbows filled with $CuSO_4$ solution. In this configuration, each elbow acted as a dummy load with an impedance that matched the 6.8Ω impedance of the OLS section of the PFL. The PFL dummy loads also served to isolate one PFL from another in the event of a LTS misfire or large OS closure timing error. While the PFL dummy loads were in place, 111 shots were fired under optimal conditions (i.e. no prefires or data loss due to scope malfunction), which corresponds to 1,332 PFL shots and 444 statistical data points when the OS data is grouped as described above.

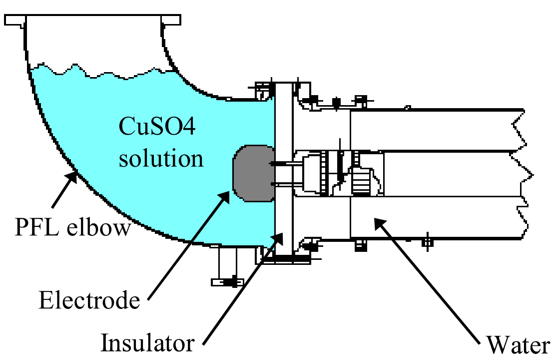

Figure 5. OS dummy load setup

During the first 64 PFL dummy load shots, OS gaps were set to 3.5cm for PFLs 1-6 and 4.0cm for PFLs 7-12 and the Marx charge was 75kV (currently the highest operating point for Mercury). These PFL dummy-load shots obtained an OS jitter below 1.2ns at the 4.0cm OS gap setting.

Jitter analysis carried out for the remaining 47 shots, which were conducted to determine the proper gap settings for each Marx charge level of interest, is summarized in Table 1. For these shots, each set of 3 commonly fed PFLs was adjusted in 1mm increments to evaluate staggering the OS gaps as a method for obtaining additional cell-to-cell delay (i.e. a 3.0cm OS gap setting corresponds to the first OS set to 2.9cm, the second set to 3.0cm, and the third set to 3.1cm). The associated 2ns/mm delay was accounted for in this analysis. At the 50-kV and 65-kV Marx charge levels, OS jitter higher than 2.0ns was noted for the OS gap settings that yielded the desired load voltage. Decreasing the gap significantly reduced the OS jitter, as shown for the 65kV case set to 3.0cm OS gap. The unexpectedly high jitter for both the 65-kV and the 50-kV cases is believed to be a result of a small sample size (only 7 shots at each charge level) and a natural consequence of reducing the voltage across the OS gaps. Electrode wear was not believed to be a problem and electrode surfaces showed even wear upon inspection. The OS jitter of 1.6ns for the 75-kv case is comparable to what was obtained in the first 64 shots.

Table 1. OS jitter for 50-kV, 65-kV, and 75-kV Marx charge levels with OS gaps staggered by 1mm

Marx Charge	<OS Jitter> [ns]		
50kV	*2.4*		
65kV	*1.0*	*2.1*	
75kV			*1.6*
OS Gap	3.0cm	3.5cm	4.0cm

C. IS Bottle Dummy Load Tests and LTS Performance

At the conclusion of the PFL dummy load tests, the measured jitter of the LTSs was 4.9ns on average. The decision was made to attempt to improve the jitter of the LTSs. The dummy loads, designed and installed between the outputs of the LTSs and the machine tank wall for initial check-out, were reinstalled. This allowed testing the LTSs without firing into the PFLs and prevented any electrode wear on the OSs.

Several steps were taken to improve LTS performance during this test series. After an optics system checkup, focusing lens replacement, and a new LTS gas fill/purge procedure, jitter at 75-kV charge voltage was reduced to ~2.0ns. This number was reduced further after uneven laser energy distribution to the LTSs was corrected by putting a lossy mirror in the trigger-laser beampath and by adjusting the pressure in the switches to account for systematic delays. Self-break pressures for 65-kV and 75-kV Marx charge levels were 7psig and 11psig respectively and a self-break condition was never observed for the 50-kV Marx charge level.

III. OVERALL SYSTEM PERFORMANCE

A. Quantifying System Performance

By using the voltage diagnostics at the OLS locations to establish a closure time for each OS (using the steepest-

slope method described previously), and accounting for the desired cell-to-cell timing delay (2 ns), a standard deviation for all 12 OS closure times can be calculated. This quantity is referred to as the combined jitter and was used as a measure of system performance from the IS bottles to the outputs of the PFLs. This quantity (calculated for each shot) represents the cumulative jitter of the LTSs, OSs, and pre-pulse switches.

B. Recent Shot Summary

Analysis was performed for all available vacuum diode shots (280-356) for 50-kV and 75-kV Marx charge. At the 50kV operating point, LTS and OS jitters of 1.1ns and 2.0ns, respectively, and a combined jitter of 2.7ns on average were obtained. At the 75-kV operating point, the LTS jitter was 1.8ns (poorer than expected), the OS jitter was 1.3ns, and the combined jitter improved to 2.4ns with respect to the 50-kV case. The OS jitter was comparable to that observed in the two previous shot ranges (results summarized in II B.). Statistics for the 75-kV operating point were calculated using a small 8 shot sample size.

Another method of quantifying system performance is to measure the jitter of the time of closure of each OS grouped by cell over all shots of interest. This analysis was completed for the same selection of shots as above and results are summarized in Table 2. As before, this analysis includes effects of all three switches (LTSs, OSs, and pre-pulse switches).

Table 2. Jitter from ideal timing per cell (ns)

	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6
75kV	*1.6*	*1.6*	*2.2*	*2.9*	*2.1*	*3.2*
50kV	*2.4*	*2.8*	*2.4*	*2.1*	*2.3*	*2.7*

C. Increasing OS Gaps to Achieve Higher Output Voltage

Several methods are available to achieve a higher output voltage. The simplest approach is to allow the PCS to charge to a higher voltage by increasing the OS gap and thereby increasing the hold-off voltage of the self-breaking OS. A simulation was run at the 75-kV operating condition where the OS closure was delayed consistent with an OS gap that was 0.5cm wider (4.5cm instead of 4.0cm). As shown in Figure 6, the resulting output pulse increased by approximately 5%. The increased stress on the stacked ring insulators and the potential increase in OS jitter caused by increasing the OS gap (as shown in the 65-kV case in Table 1) make this method of increasing the output voltage less appealing than establishing a new operating point and making corresponding hardware modifications (i.e. new OS gap settings and stacked-ring insulator modifications if deemed necessary).

IV. CONCLUSIONS

Through a series of pulsed power tests, the performance of Mercury's OSs, LTSs, and entire system from the IS bottles up to the outputs of the PFLs were quantified. LTS jitter for 75-kV charge was less than 2.0ns, which coincides with jitter values quoted for Hermes-III[4]. OS jitter between 1.2ns to 1.6ns was observed for the 75-kV charge level, which is also on the order of the jitter quoted for the OSs on Hermes-III[5]. For each operating point tested, the combined jitter was below 2.7ns. This combined jitter precludes obtaining the desired cell-to-cell 2-ns delay time. The actual timing of the cells is similar to Figure 4(b), with an appropriate spread for cells 1-3 and 4-6. The method of increasing the OS gap to achieve higher output voltage was investigated, but the risk posed by higher cell insulator stresses and possibly greater OS jitter is high for the small 5% gain in output pulse amplitude.

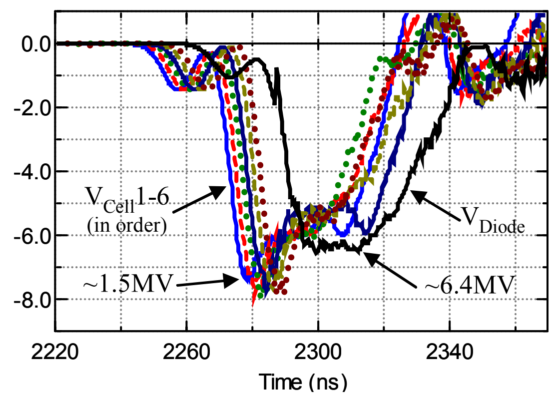

Figure 6. Simulation of voltages on cell insulator stacks and at the diode load for the 75-kV Marx charge level and 4.5-cm staggered OS gaps running self-limited.

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